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A METHOD FOR STRUCTURAL SYNTHESIS OF NETWORK CAPABLE APPLICATION PROCESSORS

I. Maykiv [1)], A. Stepanenko [1)], D. Woschall [2)]

[1)] Research Institute of Intelligent Computer Systems, Ternopil National Economic University,
46009 Ukraine, Ternopil, 11 Lvivska str.,
mim@tanet.edu.te.ua, {andrew.stepanenko@gmail.com}, http://www.ics.tneu.edu.ua/
[2)] Esensors Inc., 4240 Ridge Lea Road Suite 37 Amherst, NY 14226, USA 14226,
darold@wobschall.com, http://www.eesensors.com/

Abstract: *A method for structural synthesis of Network Capable Application Processors (NCAPs) is proposed. It is based on a method of morphological analysis and synthesis and includes phases of functional analysis, structural synthesis, and search for a set of optimal solutions. The proposed method combines lexicographical criterion of preference (L- criterion) at a stage of functional analysis and unconditional criterion of preference (Pareto optimality) during the search phase, which are considered in literature as alternative methods of search for optimal solutions. Combining of criteria, makes it possible to reduce the number of synthesized alternative variants at a stage of structural synthesis and all obtained solutions are allowable.*

Keywords: *structural synthesis, morphological analysis, lexicographical criterion of preference, unconditional criterion of preference.*

Modern measurement and control systems are implemented as multilevel systems with the distributed computing resources on the basis of industrial buses. The IEEE-1451 series of standards has been developed by IEEE for unification of requirements for hardware and software of such systems. Also a term *Network Capable Application Processor (NCAP)* as a data processing device is defined by this set of standards. NCAP occupies an intermediate level between a network server (high level) and sensors and actuators (low level). The main functions of the NCAP are data processing and support of a set of serial interfaces. However, each area of application is characterized by the set of functional tasks which demand use of the specialized device technical parameters, which are optimized for the specified area of use.

The analysis of available literature on this subject has shown, that at present the methods for optimum structural synthesis of digital systems based on microcontrollers which are characterized by a wide set of features with a significant price range is absent. The objective of this work is creation of a method for optimum structural synthesis of NCAP on the basis of microcontrollers, with optimal cost-functionality relation obtained from a set functional parameters which can appear as criterion for estimation of the device quality.

The effective technique of structural synthesis of devices with optimal cost-functionality relation includes the next stages: 1) functional analysis; 2) structural synthesis; 3) search for optimal structures. The generalized algorithm of the proposed technique includes eight stages (Fig.1) which are divided into groups: functional analysis and structural synthesis.

The requirement specification for the NCAP is analyzed at the first stage of the design process. At this stage the list of functional tasks which are executed by the NCAP is created. Functional tasks are divided on system and application tasks. System tasks are realized by operational system (OS) or the specialized software and provide interaction for the application tasks. Application tasks serve external devices and users and are divided into two groups: 1) data exchange; 2) data processing.

The analysis of application tasks is performed at the second stage. The set of information parameters necessary to make estimation on the amount of input and output data for each application task is defined as a result of the analysis. As a result of this stage a set of vectors specifying functional restrictions for the NCAP is created.

The hardware and software necessary for implementation of all application functions of system is determined at the third stage as result of the requirement specification analysis and analysis of the list of application functions executed by the NCAP.

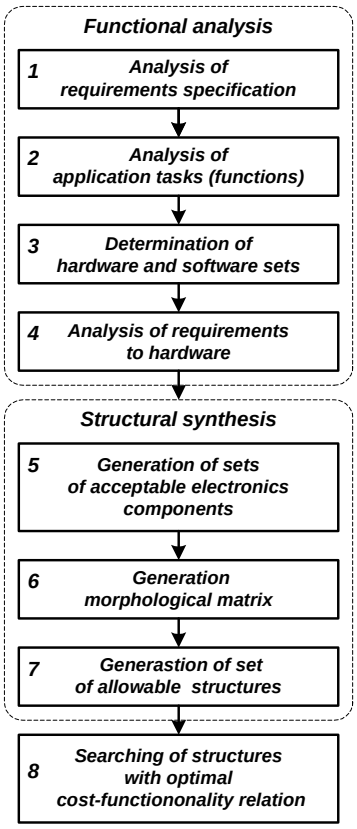

Fig.1 – Algorithm of method of structural synthesis

At the fourth stage the analysis of requirements for the device hardware is performed in particular: 1) processing power of a microcontroller; 2) memory size of ROM and RAM; 3) timing performances and temporal constraints. The estimation is made using elements of the theory of queues where the microcontroller is considered as the processing node, messages considered as service requests and message processing corresponds to service requests processing.

At the fifth stage the selection of electronic components is performed on the conducted functional analysis, where the list of the required hardware and software was created with timing characteristics and restrictions as well. The set of possible electronic components is created using lexicographic criterion of preference, which is a conditional criterion. A decision making person enters quality indicators priority list as additional information. As a result vector task of optimal selection of electronic components is transformed into a scalar task. This allows creation of a subsystem of a preliminary selection of electronic components which: 1) do not meet technical restrictions for the device being designed; 2) posses considerably better technical parameters. Such a preliminary selection enables to decrease the number of selection choices almost to the order of magnitude.

At the sixth stage a decomposition of the device into a set of basic nodes is performed using morphological method. Then a morphological matrix is created (NxM), where N is the number of basic nodes, and M is the maximum number of alternate variants of the N-th node.

At the seventh and eighth stages the set of possible device structures is generated among which the search for optimal cost-functionality combination is performed. The process of this set creation is based on principals of discrete optimization, where each node variant is characterized by implementation costs C_{nm} and functional effectiveness E_{nm}. In general for the device the following is true

$$C_\Sigma = \sum_{n=1}^{N}\sum_{m=1}^{M} C_{nm}\cdot\xi_{nm}\ ,\ E_\Sigma = \sum_{n=1}^{N}\sum_{m=1}^{M} E_{nm}\cdot\xi_{nm}$$

In this case the criterion function is described by the following equation $F_{opt} = f(C_\Sigma, E_\Sigma) \to \min$.

The known methods of bi-criterion optimization transform vector synthesis into scalar synthesis. Widespread is the search for optimal solution by:
1) resulting quality indicator as a multiply of quality criteria $k_p = C * E \to \min$ or weighted sum $k_p = (c_1 \cdot C + c_2 \cdot E) \to \min$; 2) effectiveness indicator (is considered as a function of self-cost and functional effectiveness). In this case the direct task lies in selection of a device with $E_{\min}$ and set restriction $C \le C_{\max}$, and the reverse task lies in determination of $C_{\min}$ with the set restriction $E \le E_{\max}$; 3) mini-max method.

The cost-functionality contradiction excludes the best solution by two criteria. Therefore it is useful to join the knowledge and experience of a developer with the automated synthesis of a set of not worse solutions. In this case according to the Pareto's unconditional criterion the set of not worse solutions is determined. Then, the expert selects the final solution from within this set using one conditional criterion of preference and taking into consideration technical perspectives of the device application.

As a result we have received a formal solution of the discrete optimization task for design of digital structures based on microcontrollers. This solution is universal for a wide set of optimization tasks.

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