

computing@computingonline.net www.computingonline.net

ISSN 1727-6209 International Journal of Computing

RECONFIGURABLE CELL-ARRAY (RCA) BASED COMPUTER SYSTEM WITH CELL SPECIALIZATION

Anatoliy Bilenko, Valeriy Sitnikov

Odessa National Polytechnic University, 1, Shevchenko avenue, Odessa, 65044, Ukraine, anatoliy.bilenko@gmail.com

Abstract: Reconfigurable system based on cell specialization of reconfigurable cell-array computer system is presented. Analysis of specialized reconfigurable cell-array hardware and methods of specialized cell inclusion are given.

Keywords: architecture of computer systems, reconfigurable systems.

Development of reconfigurable computing systems is characterized by a rapid increase in computational complexity. This leads to the problem of optimal use of hardware resources of ICs, reconfigurable system is based on.

Significant contribution to the development of methods and means of reconfigurable computing design was introduced by ukraininan and foreign scientiests, such as A.O. Melnik, A. Palagin, V.N. Opanasenko, I.A. Kaliayev, I. Levine, E. Semernikov, V.I. Shmoylov, G. Estrin, S. Hauck, D. Patterson. Several scientific researches [1-3] reveal approaches to implementation of the reconfigurable systems, based on FPGAs. Other papers [4,5] show approaches, based on additional hardware reconfiguration.

In this paper an approach to the implementation of reconfigurable computing based on the introduction of additional hardware layer "on top of FPGAs" is reviewed.

Existing specialized units in the FPGA, sets the problem of optimal inclusion of these resources into the reconfigurable system.

Reconfigurable computing unit (RCU) of the RCA consists of a computational cells, connected with other cells of the vertical and horizontal connections, which can significantly save on the number of connections, which increases the reliability of the system, and this structure makes it possible for microelectronic realization.

The need to optimize the utilization of existing specialized units of FPGA leads to the statement of the problem of RCU structure specialization.

The choice of the structure of RCA cell is

performed according to the constraints imposed by the a given computational task. Obviously, the cell must be optimized to perform operations which are most commonly used in the computation process. The problem of the specialization of cells arises from the mismatch of operations implemented in RCA and RCA cell architecture.

It is proposed to modify the structure of RCU so that use a limited number of specialfuction units of FPGA. However, specialization should not significantly affect the structure of the RCU, as well as the developed software. Considering listed requirements and restrictions, it is proposed to modify the structure of the RCU as follows: in each row of the matrix included specialized ALU, which is shared between all the cells in that line. Accordingly, ALU sharing algorithms need to be run before the reconfiguration stage of the system.

In general, the problem of optimal inclusion and selection of specialized cells for RCU is a combinatorial search of the cells placement variants.

A typical time it takes to trace and place cells of data flow graph (DFG) is measured in tens of seconds, and increases with the size of DFG and the structure of the RCU. This is not acceptable for modern computing systems.

Effectiveness of computer networks and its nodes utilization can be modeled with maximal flow function on the network graph. Performance of the system can be measured by critical path function of the network graph.

While preparation to the stage of RCU structure optimization, it's needed to find optimal operations for given computational task. Such operations

should be included into ALU of RCU. For example, fig. 1 shows typical DFG of operations used in DSP computational tasks.

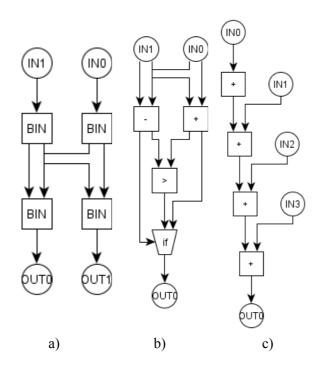


Fig. 1 – DFGs of computational tasks in DSP: a) FFT; b), absolute difference; c) filtering

Selection of the optimal replacement set of the DFG vertices is produced on the basis of optimality criteria and imposed restrictions, represented in the system (1):

$$\begin{cases} \max_{w \in W_g} (\alpha_1 \cdot \Phi(w) + \alpha_2 \cdot \Psi(w)) \\ \alpha_1 + \alpha_2 = 1 \\ w_i \in W_g, i = 1, N \end{cases}$$

$$\sum_{i=1}^{N} w_i = N \cdot w_0$$
(1)

where $\Phi(w)$ is a maximum flow function of its DFG, $\Psi(w)$ is a function of critical path of given DFG, N- number of RCU cells to replace by specialized cells, w_0 – starting weight of DFG edge.

Once the solution of system (1) is obtained, DFG edges weight analysis is performed. The variants for placement of specialized ALUs are the cells that are connected by edges of maximum weight.

In the article an approach to specialization of RCU of RCA is reviewed. The task of structure optimization is set. Details of planning and organization of RCU structure is shown.

REFERENCES

- [1] A. Palagin, V. N. Opanasenko, Design of reconfigurable FPGA devices, *Radioelektronic and computer systems*, (6) (2008), pp. 257-260. (in Russian).
- [2] A. A. Melnik, A. M. Salo, V. A. Klimenko, L. A. Tsyhylyk, A. Yurchuk, Implementation of software specialized processors in reconfigurable accelerators of universal PC, Bulletin of National. University "Lvivska politehnika" Computer Systems and Networks, (658) (2009). (in Ukrainian)
- [3] A. A. Melnik, I. D. Yakovlev, Comparative analysis of methods of matrix representation of algorithms' graphs, Bulletin of National University "Lvivska politehnika" Computer Systems and Networks, (658) (2009), pp. 78-84. (in Ukrainian)
- [4] Kaliayev I. A., Levin I. I., Semernikov E. A., Shmoylov V. I., *Reconfigurable computing based on multi-pipeline structures*, Rostov on Don SSC RAN Academy of Sciences, 2008, 393 p. (in Russian)
- [5] N. Lukin, Fundamentals of the theory of architecture design of functional-oriented processors for real-time, *High-performance computing systems, Proceedings of the Fifth International Workshop on Modern School and the Fifth International Youth Science and Engineering Conference,* August 31 September 6, 2008, Taganrog Taganrog Iss. TTI SFU, 2008, pp. 115-166. (in Russian)
- [6] LogiCORE IP DSP48 Macro v2.0. web-link: http://www.xilinx.com/support/documentation/ip_documentation/dsp48_macro_ds754.pdf
- [7] DSP Blocks in Stratix & Stratix GX Devices. web-link: http://www.altera.com/literature/hb/stx/ch_6_vol_2.pdf
- [8] Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, Clifford Stein, Introduction to Algorithms, (third ed.), MIT Press, 2009.